

# **DDR2 Un-buffered/ECC DIMM Module**

**1GB based on 512Mbit component**

**72-bit ECC**

**60 Balls FBGA with Pb-Free**



**Revision 1.0 (Mar. 2006)**  
-Initial Release

**1.0 Feature**

- JEDEC standard 1.8V +/- 0.1V Power Supply
- Standard Double-Data-Rate-Two Synchronous DRAMs with single 1.8V power supply
- Programmable CAS latencies (3,4,5,6), Burst Length (4 & 8) and Burst Type (Sequential / Interleave)
- Auto Refresh (CRB) and Self Refresh
- Bi-directional Differential Data Strobe (Single ended data strobe is option)
- Off Chip Driver (OCD) impedance adjustment
- On-Die termination with selectable values (50/75/150 ohms or disable)
- PASR (Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C - support High Temperature Self-Refresh rate enable feature
- Serial presence detect with EEPROM
- DIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- All speed grades faster than DDR400 comply with DDR400 timing specifications
- Based on JEDEC standard reference Raw Cards Lay out.
- Package: 60ball FBGA - 64Mx8
- RoHS compliant
- Gold plated contacts

**2.0 Ordering Information**

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
T800EB1G/S	1GB	128Mx72	64Mx8	FBGA	2	1GB 2Rx8 PC2-6400R

**3.0 Operating Frequencies**

	DDR2-800	DDR2-667	DDR2-533	DDR-400	Unit
Speed @ CL3	-	400	400	400	Mbps
Speed @ CL4	400	533	533	400	Mbps
Speed @ CL5	533	667	533	-	Mbps
Speed @ CL6	800	-	-	-	Mbps
CL-tRCD-tRP	6-6-6	5-5-5	4-4-4	3-3-3	CK

**4.0 Absolute Maximum DC Rating**

Symbol	Parameter	Rating	Units
V <sub>in</sub> , V <sub>out</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5 ~ 2.3	V
V <sub>DD</sub>	Voltage on V <sub>DD</sub> & V <sub>DDQ</sub> supply relative to V <sub>SS</sub>	-1.0 ~ 2.3	V
V <sub>DDQ</sub>	Short circuit current	-0.5 ~ 2.3	V
V <sub>DDL</sub>	Power dissipation	-0.5 ~ 2.3	V
T <sub>STG</sub>	Storage Temperature	-55 ~ + 100	°C

**5.0 DIMM Pin Configurations (Front side/Back side)**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V <sub>REF</sub>	121	V <sub>SS</sub>	31	DQ19	151	V <sub>SS</sub>	61	A4	181	V <sub>DDQ</sub>	91	V <sub>SS</sub>	211	DM5
2	V <sub>SS</sub>	122	DQ4	32	V <sub>SS</sub>	152	DQ28	62	V <sub>DDQ</sub>	182	A3	92	$\overline{\text{DQS5}}$	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V <sub>SS</sub>
4	DQ1	124	V <sub>SS</sub>	34	DQ25	154	V <sub>SS</sub>	64	V <sub>DD</sub>	184	V <sub>DD</sub>	94	V <sub>SS</sub>	214	DQ46
5	V <sub>SS</sub>	125	DM0	35	V <sub>SS</sub>	155	DM3	<b>KEY</b>				95	DQ42	215	DQ47
6	$\overline{\text{DQS0}}$	126	NC	36	$\overline{\text{DQS3}}$	156	NC	65	V <sub>SS</sub>	185	CK0	96	DQ43	216	V <sub>SS</sub>
7	DQS0	127	V <sub>SS</sub>	37	DQS3	157	V <sub>SS</sub>	66	V <sub>SS</sub>	186	$\overline{\text{CK0}}$	97	V <sub>SS</sub>	217	DQ52
8	V <sub>SS</sub>	128	DQ6	38	V <sub>SS</sub>	158	DQ30	67	V <sub>DD</sub>	187	V <sub>DD</sub>	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC/Par_in	188	A0	99	DQ99	219	V <sub>SS</sub>
10	DQ3	130	V <sub>SS</sub>	40	DQ27	160	V <sub>SS</sub>	69	V <sub>DD</sub>	189	V <sub>DD</sub>	100	V <sub>SS</sub>	220	RFU
11	V <sub>SS</sub>	131	DQ12	41	V <sub>SS</sub>	161	CB4	70	A10/AP	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V <sub>DDQ</sub>	102	NC(Test)	222	V <sub>SS</sub>
13	DQ9	133	V <sub>SS</sub>	43	CB1	163	V <sub>SS</sub>	72	V <sub>DDQ</sub>	192	$\overline{\text{RAS}}$	103	V <sub>SS</sub>	223	DM6
14	V <sub>SS</sub>	134	DM1	44	V <sub>SS</sub>	164	DM8	73	$\overline{\text{WE}}$	193	S0	104	$\overline{\text{DQS6}}$	224	NC
15	$\overline{\text{DQS1}}$	135	NC	45	$\overline{\text{DQS8}}$	165	NC	74	$\overline{\text{CAS}}$	194	V <sub>DDQ</sub>	105	DQS6	225	V <sub>SS</sub>
16	DQS1	136	V <sub>SS</sub>	46	DQS8	166	V <sub>SS</sub>	75	V <sub>DDQ</sub>	195	ODT0	106	V <sub>SS</sub>	226	DQ54
17	V <sub>SS</sub>	137	RFU	47	V <sub>SS</sub>	167	CB6	76	S1	196	A13	107	DQ50	227	DQ55
18	$\overline{\text{RESET}}$	138	RFU	48	CB2	168	CB7	77	ODT1	197	V <sub>DD</sub>	108	DQ51	228	V <sub>SS</sub>
19	NC	139	V <sub>SS</sub>	49	CB3	169	V <sub>SS</sub>	78	V <sub>DDQ</sub>	198	V <sub>SS</sub>	109	V <sub>SS</sub>	229	DQ60
20	V <sub>SS</sub>	140	DQ14	50	V <sub>SS</sub>	170	V <sub>DDQ</sub>	79	V <sub>SS</sub>	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V <sub>DDQ</sub>	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V <sub>SS</sub>
22	DQ11	142	V <sub>SS</sub>	52	CKE0	172	V <sub>DD</sub>	81	DQ33	201	V <sub>SS</sub>	112	V <sub>SS</sub>	232	DM7
23	V <sub>SS</sub>	143	DQ20	53	V <sub>DD</sub>	173	NC	82	V <sub>SS</sub>	202	DM4	113	$\overline{\text{DQS7}}$	233	NC
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{\text{DQS4}}$	203	NC	114	DQS7	234	V <sub>SS</sub>
25	DQ17	145	V <sub>SS</sub>	55	NC/Err_Out	175	V <sub>DDQ</sub>	84	DQS4	204	V <sub>SS</sub>	115	V <sub>SS</sub>	235	DQ62
26	V <sub>SS</sub>	146	DM2	56	V <sub>DDQ</sub>	176	A12	85	V <sub>SS</sub>	205	DQ38	116	DQ58	236	DQ63
27	$\overline{\text{DQS2}}$	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V <sub>SS</sub>
28	DQS2	148	V <sub>SS</sub>	58	A7	178	V <sub>DD</sub>	87	DQ35	207	V <sub>SS</sub>	118	V <sub>SS</sub>	238	V <sub>DDSPD</sub>
29	V <sub>SS</sub>	149	DQ22	59	V <sub>DD</sub>	179	A8	88	V <sub>SS</sub>	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V <sub>SS</sub>				

NC = No Connect, RFU = Reserved for Future Use

1. Pin 196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

**6.0 Dimm Pin Description**

Pin Name	Function	Pin Name	Function
A0 ~ A9, A11~A13	Address input (Multiplexed)	ODT0~ODT1	On Die Termination
A10/AP	Address Input/Auto pre-charge	CB0~CB7	Data check bits Input/Output
BA0 ~ BA2	Bank Select	DQ0~DQ63	Data Input/Output
$\overline{CK0}$ ~ $\overline{CK2}$ , CK0~CK2	Clock input	$\overline{DQS0}$ ~ $\overline{DQS8}$	Data strobes, negative line
CKE0, CKE1	Clock enable input	DM (0~8),	Data Masks/Data strobes (Read)
$\overline{S0}$ , $\overline{S1}$	Chip select input	DQS0~DQS8	Data Strobes
$\overline{RAS}$	Row address strobe	RFU	Reserved for future used
$\overline{CAS}$	Column address strobe	NC	No connection
$\overline{WE}$	Write Enable	TEST	Memory bus test tool
SCL	SPD Clock Input	V <sub>DD</sub>	Core Power
SDA	SPD Data Input/Output	V <sub>DDQ</sub>	I/O Power
SA0~SA2	SPD Address	V <sub>SS</sub>	Ground
Par_In	Parity bit for address & Control bus	V <sub>REF</sub>	Input/Output Reference
Err_Out	Parity error found in the Address and Control bus	V <sub>DDSPD</sub>	Serial EEPROM Power/Supply
$\overline{Reset}$	Register and PLL control pin		

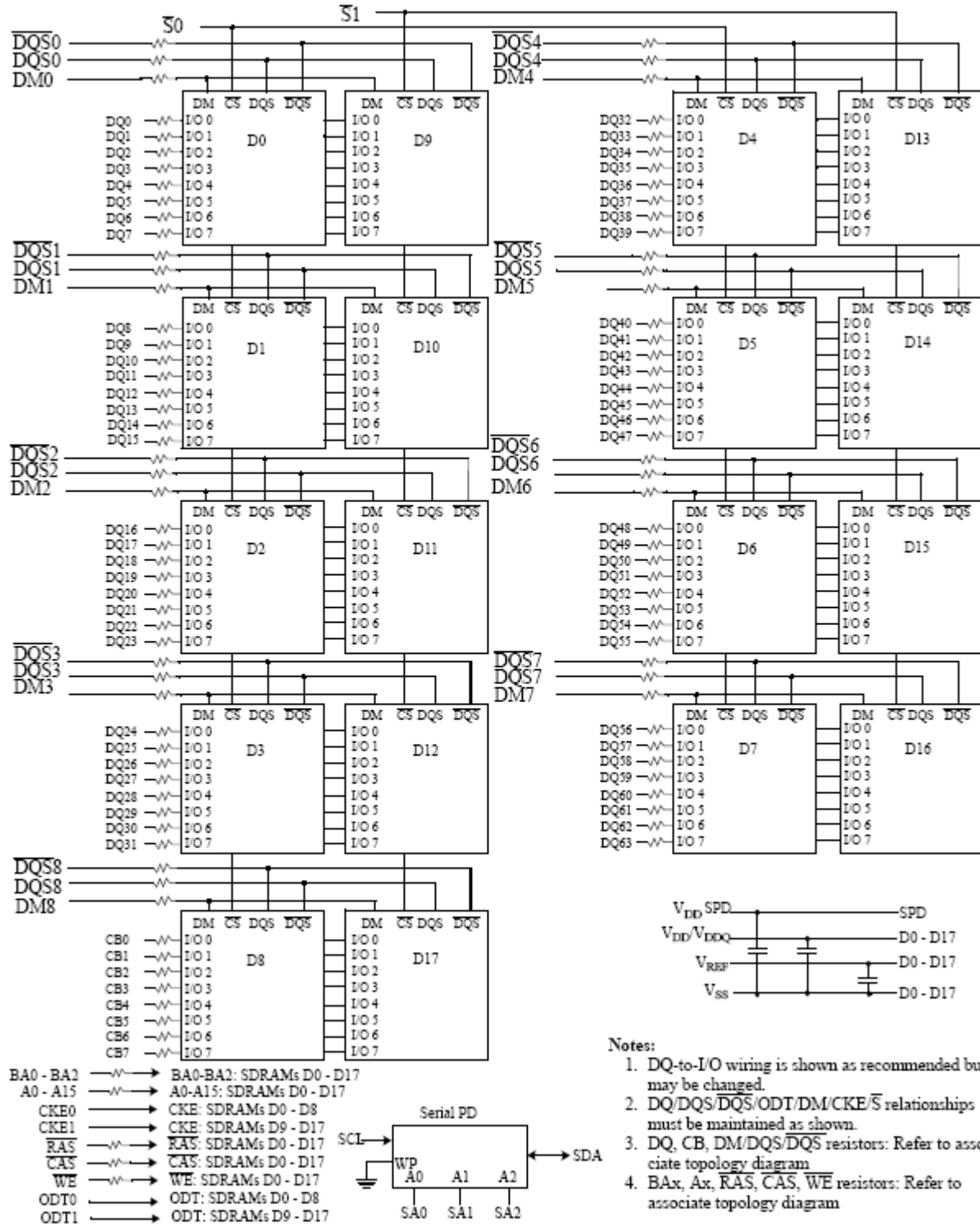
**7.0 Address Configuration**

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
64Mx8(512Mb) base	A0-A13	A0-A9	BA0-BA1	A10

**240-Pin Un-buffered/ECC DIMM**

**DDR2 SDRAM**

**8.0 Functional Block Diagram: 1GB, 128Mx72 Module (Populated as 2 ranks of x8 SDRAM DDR2 Module)**



**9.0 AC & DC Operating Conditions**

Recommended operating conditions (Voltage referenced to V<sub>SS</sub>=0V, T<sub>A</sub>=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage	1.7	1.8	1.9	V
V <sub>DDL</sub>	Supply Voltage for DLL	1.7	1.8	1.9	V
V <sub>DDQ</sub>	Supply Voltage for Output	1.7	1.8	1.9	V
V <sub>REF</sub>	Input Reference Voltage	0.49*V <sub>DDQ</sub>	0.50*V <sub>DDQ</sub>	0.51*V <sub>DDQ</sub>	mV
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V

**10.0 Capacitance(Max.)**

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

**11.0 AC Timing Parameters & Specifications**

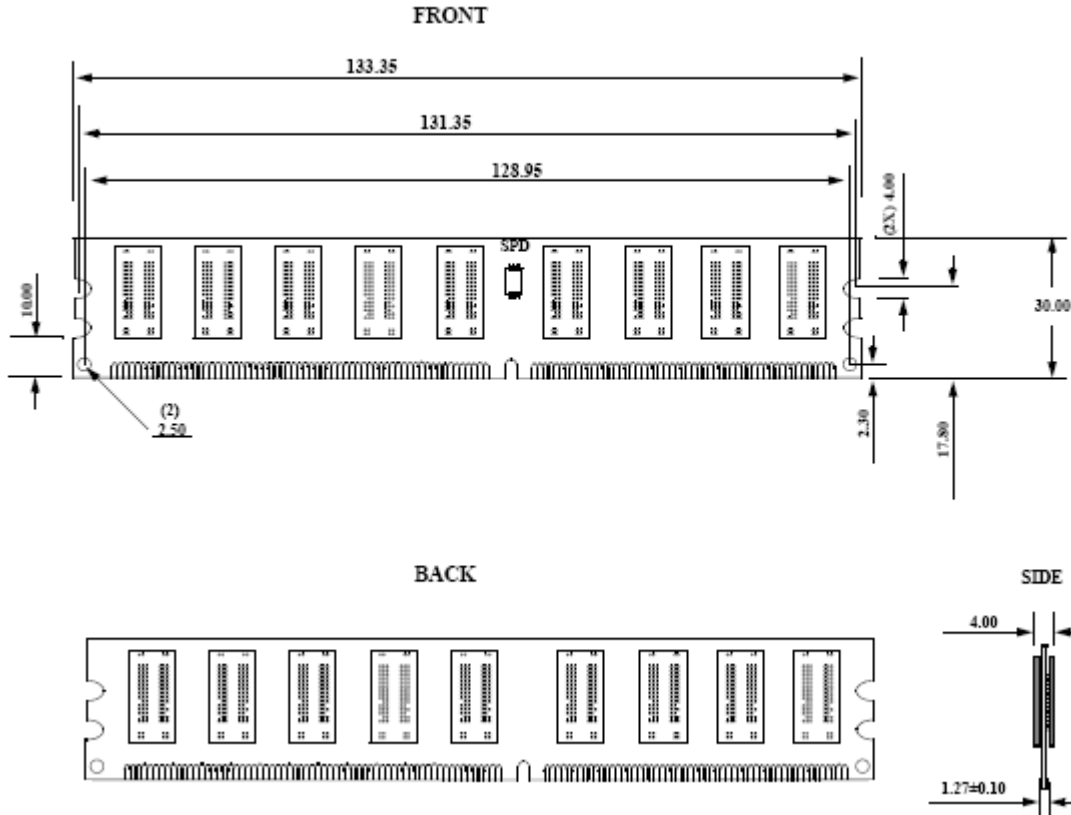
(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQ output access time from CK/ $\overline{CK}$	t <sub>AC</sub>	-400	+400	-450	+450	-500	+500	-600	+600	ps
DQS output access time from CK/ $\overline{CK}$	t <sub>DQSCK</sub>	-350	+350	-400	+400	-450	+450	-500	+500	ps
CK high-level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK half period	t <sub>HP</sub>	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	min(t <sub>CL</sub> , t <sub>CH</sub> )	x	ps
Clock cycle time, CL=x	t <sub>CK</sub>	2500	8000	3000	8000	3750	8000	5000	8000	ps
DQ and DM input hold time	t <sub>DH</sub> (base)	125	x	175	x	225	x	275	x	ps
DQ and DM input setup time	t <sub>DS</sub> (base)	50	x	100	x	100	x	150	x	ps
Control & Address input pulse width for each input	t <sub>IPW</sub>	0.6	x	0.6	x	0.6	x	0.6	x	tCK
DQ and DM input pulse width for each input	t <sub>DIPW</sub>	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Data-out high-impedance time from CK/ $\overline{CK}$	t <sub>HZ</sub>	x	t <sub>AC</sub> max	x	t <sub>AC</sub> max	x	t <sub>AC</sub> max	x	t <sub>AC</sub> max	ps
DQS low-impedance time from CK/ $\overline{CK}$	t <sub>LZ</sub> (DQS)	t <sub>AC</sub> min	t <sub>AC</sub> max	t <sub>AC</sub> min	t <sub>AC</sub> max	t <sub>AC</sub> min	t <sub>AC</sub> max	t <sub>AC</sub> min	t <sub>AC</sub> max	ps
DQ low-impedance time from CK/ $\overline{CK}$	t <sub>LZ</sub> (DQ)	2*t <sub>AC</sub> min	t <sub>AC</sub> max	2*t <sub>AC</sub> min	t <sub>AC</sub> max	2*t <sub>AC</sub> min	t <sub>AC</sub> max	2*t <sub>AC</sub> min	t <sub>AC</sub> max	ps
DQS-DQ skew for DQS and associated DQ signals	t <sub>DQSQ</sub>	x	200	x	240	x	300	x	350	ps
DQ hold skew factor	t <sub>QHS</sub>	x	300	x	340	x	400	x	450	ps
DQ/DQS output hold time from DQS	t <sub>QH</sub>	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	t <sub>HP</sub> - t <sub>QHS</sub>	x	ps
First DQS latching transition to associated clock edge	t <sub>DQSS</sub>	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK

Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units
		min	max	min	max	min	max	min	max	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	0.35	x	tCK
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	0.2	x	tCK
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	0.2	x	tCK
Mode register set command cycle time	tMRD	2	x	2	x	2	x	2	x	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	0.35	x	tCK
Address and control input hold time	tIH(base)	250	x	275	x	375	x	475	x	ps
Address and control input setup time	tIS(base)	175	x	200	x	250	x	350	x	ps
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	7.5	x	ns
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	10	x	ns
Four Activate Window for 1KB page size products	tFAW	35		37.5		37.5		37.5		ns
Four Activate Window for 2KB page size products	tFAW	45		50		50		50		ns
CAS to CAS command delay	tCCD	2	x	2		2		2		tCK
Write recovery time	tWR	15	x	15	x	15	x	15	x	ns
Auto pre-charge write recovery + pre-charge time	tDAL	WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK
Internal write to read command delay	tWTR	7.5		7.5	x	7.5	x	10	x	ns
Internal read to pre-charge command delay	tRTP	7.5		7.5		7.5		7.5		ns
Exit self refresh to a non-read command	tXSNRt	tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns
Exit self refresh to a read command	tXSRD	200		200		200		200		tCK
Exit pre-charge power down to any non-read command	tXP	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command	tXARD	2	x	2	x	2	x	2	x	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL		7 - AL		6 - AL		6 - AL		tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		3		3		tCK
ODT turn-on delay	tAOND	2	2	2	2	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(max) + 1t	tAC(min)	tAC(max) + 1t	ns
ODT turn-on (Power-Down mode)	tAONPD	tAC(min) + 2	2tCK+tAC(max)+1	tAC(min) + 2	2tCK+tAC(max)+1	tAC(min) + 2	2tCK+tAC(max)+1	tAC(min) + 2	2tCK+tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min) + 2	2.5tCK + tAC(max)+1	tAC(min) + 2	2.5tCK + tAC(max)+1	tAC(min) + 2	2.5tCK + tAC(max)+1	tAC(min) + 2	2.5tCK + tAC(max)+1	ns
ODT to power down entry latency	tANPD	3		3		3		3		tCK
ODT power down exit latency	tAXPD	8		8		8		8		tCK
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK + tIH		tIS+tCK + tIH		tIS+tCK + tIH		tIS+tCK + tIH		ns

**12.0 Physical Dimensions: (64Mx8 Based)  
128Mx72 (2 Ranks)**

Units : Millimeters



Tolerances : ± 0.005(.13) unless otherwise specified